DAVID KUAN-YU LIU, Ph.D.

42063 Benbow Drive, Fremont, CA 94539 ● (510) 770-9449 or (510) 579-5029
www.davidkyliu.com davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Consultant and expert witness for semiconductor intellectual property evaluation and patent litigation, with successful deposition experience.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

EXPERT WORK EXPERIENCE:

Case:	**Ziptronix vs. TSMC**
Jurisdiction:	Ziptronix patent IPR work
Work Product:	Testifying expert, claim chart analysis, researching prior art for invalidity arguments, and claim chart with prior art assessment
Nature of Case:	Representing TSMC. IPR review of possible patents asserted against TSMC.
Counsel:	Retained by Fish Richardson (Contact: John Goetz)
Date:	7/15 – 1/16

Case:	**Triune Systems, LLC vs. Wayne Chen, et al.,**
Jurisdiction:	Cause No. 296-03209-2013, 296 District Court of Collin County, TX United States International Trade Commission
Work Product:	Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case:	Representing Wayne Chen. Defending against trade secret contention.
Counsel:	Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date:	5/15 – 9/15

Case:	**Macronix vs. Spansion**
Jurisdiction:	Investigation No. 337-TA-922 United States International Trade Commission
Work Product:	Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case:	Representing Macronix. ITC infringement case concerning Flash memory cell
Counsel:	Retained by Fish Richardson (Contact: David Barken)
Date:	9/14 – 1/15

Case:	**Macronix vs. Spansion**
Jurisdiction:	Investigation No. 337-TA-909 United States International Trade Commission
Work Product:	Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case:	Representing Macronix. ITC infringement case concerning Flash memory cell
Counsel:	Retained by Winston & Strawn (Contact Michael Murray)
Date:	5/14 – 1/15

Case:	**Keranos, LLC v. Analog Devices et. al.**
Jurisdiction:	Civil Case No. 2:10-CV-00207 United States District Court for the Eastern District of Texas
Work Product:	Claim Chart Generation and Claim Construction
Nature of Case:	Representing Keranos, LLC. Patent infringement case concerning split gate Flash memory cell
Counsel:	Retained by Agility IP (Contact Michelle Breit)
Date:	2/09 – 2/14

Case:	**Silicon Storage Technology, Inc. v. Xicor, LLC**
Jurisdiction:	Civil Case No. CV 10-01515 United States District Court for the Northern District of California
Work Product:	Expert report, and declarations
Nature of Case:	Representing Xicor concerning United States Reissue Patent RE38,370 on the process of flash memory cell.

Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: **Fast Memory Erase, LLC v. Spansion et.al.**
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Representing Fast Memory Erase, LLC. In defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: **Fast Memory Erase, LLC v. Spansion et.al.**
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Expert report, declarations, and depositions
Nature of Case: Representing Fast Memory Erase, LLC. Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant**

Gordon & Rees LLP, Served as a testifying expert for trade secret contention case of Triune Systems vs. Wayne Chen, *et al*., Case ended in settlement after summary jury trial. Responsible for gathering and reviewing of evidence, analyzed integrated circuits for technology features, issuing expert report, and video taped jury trial testimony.

Fish & Richardson, Served as a testifying expert for the case of Macronix vs. Spansion. Case ended in settlement. Responsible for gathering and reviewing of evidence, both for DI purpose and for infringement purpose, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report.

Winston & Strawn. Served as a consulting expert for the case of Macronix vs. Spansion. Case ended in settlement. Responsible for gathering and reviewing of evidence, both for DI purpose and for infringement purpose.

ShoreChanBragalone. Served as an expert witness for the case of Intersil vs. SST. Summary judgment was granted after claim charts and infringement contention were generated.

Keranos, Serving as an expert witness for the case of Keranos, LLC vs. Analog Devices, Inc. et. al. Overseeing the generation of claim charts and coordinating efforts in reverse engineering work on integrated circuit products.

ShoreChanBragalone. Served as an expert witness and testifying witness for the case of Fast Memory Erase, LLC *vs*. Spansion *et al*. (Performed claim construction, provided deposition testimony, and wrote expert report.)

RPX Corporation. Evaluated flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent (total 76 patents) and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets.

IBM Corp. Reviewed and evaluated IBM's 180nm HV process technology against customer's IP and applications, with a view toward IBM's potential bid for customer's process technology offerings. Assessed process compatibility and outlined gap/overlaps between IBM and customer.

Law+. Worked as a technical expert for the lead attorney on several IP litigation cases in the area of flash memory and CMOS process technology. Assembled critical evidence to invalidate key patent claims. Generated claim charts for several patents.

10/07 to 4/11: **Jonker, LLC**
Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**
Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35μm and 0.18μm CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**
Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**
Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00 **Programmable Silicon Solutions, Sunnyvale, California**
Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98 **AMIC Technology, Santa Clara, California**
Director of Flash Technology. Responsible for developing 0.35μm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97 **Altera Corp., San Jose, California**
Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35μm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96 **Information Storage Devices, San Jose, California**
Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95 **Advanced Micro Devices, Sunnyvale, California**
Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5μm and 0.35μm flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92 **Texas Instruments, Dallas, Texas**

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983
AEA Faculty Development Fellowship, 1983-1985
AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, “Programmable Gate Array and Methods for Its Fabrication” (with K-L. Chen and H. Tigelaar), issued April 21, 1992.

2. U.S. Patent 5,166,557, “Gate Array with Built-in Programmable Circuitry” (with K.-L. Chen), issued November 24, 1992.

3. U.S. Patent 5,202,576, “Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same” (with M. Wong), issued April 13, 1993.

4. U.S. Patent 5,219,782, “Sublithographic Antifuse and method for Manufacturing” (with K.-L. Chen), issued June 15, 1993.

5. U.S. Patent 5,250,464, “Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure” (with M. Wong), issued October 5, 1993.

6. U.S. Patent 5,264,384, “Method of Making a Non-Volatile Memory Cell” (with C. Kaya), issued November 23, 1993.

7. U.S. Patent 5,300,803, “Source Side Injection Non-volatile Memory Cell,” issued April 5, 1994.

8. U.S. Patent 5,365,105, “Sidewall Antifuse Structure and Method for Making,” issued November 15, 1994.

9. U.S. Patent 5,371,402, “Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process” (with M. Wong), issued December, 1994

10. U.S. Patent 5,395,797, “Antifuse Structure and Method of Fabrication,” issued March 7, 1995.

11. U.S. Patent 5,470,773, “Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch” (with Y. Sun and C. Chang), issued November 28, 1995.

12. U.S. Patent 5,482,880, “Non-Volatile Memory and Fabrication Method,” (with C. Kaya), issued January 9 1996.

13. U.S. Patent 5,517,443, “Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device,” issued May 14, 1996.

14. U.S. Patent 5,521,867, “Adjustable Threshold Voltage Conversion Circuit” (with Jian Chen), issued May 28, 1996.

15. U.S. Patent 5,534,455, “Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device,” issued July 9, 1996.

16. U.S. Patent 5,541,875, “High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array” (with Jian Chen), issued May 28, 1996.

17. U.S. Patent 5,590,076, “Channel Hot-Carrier Page Write,” issued December 31, 1996.

18. U.S. Patent 5,596,531, “Method for Decreasing the Discharge Time of A Flash Memory Cell,” issued January 21, 1997.

19. U.S. Patent 5,612,914, “Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same” (with Man Wong), issued May 18, 1997.

20. U.S. Patent 5,624,859, “Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device,” issued April 29, 1997.

21. U.S. Patent 5,625,220, “Sublithographic Antifuse,” (with K.L. Chen), issued April 29, 1997.

22. U.S. Patent 5,646,430, “Non-volatile Memory Cell Having Lightly-Doped Source Region” (with C. Kaya), Issued July 8, 1997.

23. U.S. Patent 5,650,964, “Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge,” (with Jian Chen), Issued July 22, 1997.

24. U.S. Patent 5,652,155, “Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant,” Issued July 27, 1997.

25. U.S. Patent 5,656,509, “Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch,” Issued July 29, 1997

26. U.S. Patent 5,661,059, “Boron Penetration to Suppress Short Channel Effect in P-channel Device,” Issued August 26, 1997.

27. U.S. Patent 5,674,764, “Method of Making Asymmetrical Non-volatile Memory Cell,” Issued October 7, 1997.

28. U.S. Patent 5,693,972, “Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device,” Issued December 2, 1997.

29. U.S. Patent 5,751,631, “Flash memory cell and a new method for sensing the content of the new memory cell,” Issued May 12, 1998

30. U.S. Patent 5,789,295, “Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process,” Issued August 4, 1998.

31. U.S. Patent 5,814,854, “Highly scalable FLASH EEPROM cell,” Issued September 29, 1998.

32. U.S. Patent 5,814,864, “Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant,” Issued September 29, 1998.

33. U.S. Patent 5,912,836, “Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array,” Issued June 15, 1999.

34. U.S. Patent 5,930,174, “Circuit and Method for Erasing Flash Memory Array,” Issued July 27, 1999.

35. U.S. Patent 5,981,994, “Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements,” Issued November 9, 1999.

36. U.S. Patent 5,995,418, “Circuit and Method for Erasing Flash Memory Array,” Issued November 30, 1999.

37. U.S. Patent 6,026,017, “Compact nonvolatile memory,” Issued February 15, 2000.

38. U.S. Patent 6,027,974, “Nonvolatile memory,” Issued February 22, 2000.

39. U.S. Patent 6,088,263, “Non-volatile memory using substrate electrons,” Issued July 11, 2000.

40. U.S. Patent 6,091,636, “Flash memory cell and a new method for sensing the content of the new memory cell,” Issued July 18, 2000.

41. U.S. Patent 6,127,225, “Memory cell having implanted region formed between select and sense transistors,” Issued October 3, 2000.

42. U.S. Patent 6,159,800, “Method of forming memory cell,” Issued December 12, 2000.

43. U.S. Patent 6,188,604, “Flash memory cell & array with improved pre-program and erase characteristics,” Issued February 13, 2001.

44. U.S. Patent 6,185,133, “Flash EPROM using junction hot hole injection for erase,” Issued February 6, 2001.

45. U.S. Patent 6,252,799, “Device with embedded Flash and EERPOM memories,” Issued June 26, 2001.

46. U.S. Patent 6,326,265, “Device with Embedded Flash and EPROM Memories,” Issued December 4, 2001.

47. U.S. Patent 6,417,550, “High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage,” Issued July 9, 2002.

48. U.S. Patent 6,479,862, “Charge trapping device and method for implementing a transistor having a negative differential resistance mode,” Issued November 12, 2002.

49. U.S. Patent 6,512,274, “CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same,” Issued January 28, 2003.

50. U.S. Patent 6,596,617, “CMOS compatible process for making a tunable negative differential resistance (NDR) device,” Issued July 22, 2003.

51. U.S. Patent 6,624,026, “Nonvolatile Memory,” Issued September 23, 2003.

52. U.S. Patent 6,680,245, “Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process,” Issued January 20, 2004.

53. U.S. Patent 6,686,631, “Negative differential resistance (NDR) device and method of operating same,” Issued February 3, 2004.

54. U.S. Patent 6,693,027, “Method for configuring a device to include a negative differential resistance (NDR) characteristic,” Issued February 17, 2004.

55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.

57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.

58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.

59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.

60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.

61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.

62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.

63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.

64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.

65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.

66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.

67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.

68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.

69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010

70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.

71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.

72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010

73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010

75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011

76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011

77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011

78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012

79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012

80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012

81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012

82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.

83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Noon-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.

84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.

85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.

86. U.S. Patent 8,705,263 "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.

87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.

88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.

(additional patent applications pending)

PUBLICATIONS

1. S.D. Leeke, D. K. Y. Liu and J. P. McVittie, "Plasma mode trench etching with direct hydrocarbon injection," *Materials Research Society Symposium Proceedings*, Vol. 68, pp. 21-27, 1986.
2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
9. K. T. San, C. Kaya, D. K. Y. Liu, T. P. Ma, and P. Shah, "A new technique for determining capacitive coupling coefficients in flash EPROMs," *IEEE Electron Device Letters*, Vol. 13, No. 6, pp. 328-331, 1992.
10. C. Kaya, D. K. Y. Liu, J. Paterson and P. Shah, "Buried source-side injection (BSSI) for flash EPROM programming," *IEEE Electron Device Letters*, Vol. 13, No. 9, pp. 465-467, 1992.
11. M. Wong, D. K. Y. Liu and S. S.-W. Huang, "Analysis of the subthreshold slope and the linear transconductance techniques for the extraction of the capacitance coupling coefficients of floating-gate devices," *IEEE Electron Device Letters*, Vol. 13, No. 11, pp. 566-568, 1992.
12. D. K. Y. Liu and J. D. Plummer, "Design and analysis of a new conductivity-modulated power MOSFET," *IEEE Transactions on Electron Devices*, Vol. 40, No. 2, pp. 428-438, 1993.
13. J. Z. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, Y. Sun, D. Liu, Y. Tang, J. Hsu, S. Luan, J. Lien, "Flash EPROM endurance simulation using physics-based models," In *International Electron Devices Meeting Technical Digest*, pp. 295-298, 1994.
14. J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, "Short Channel enhanced degradation during discharge of Flash EEPROM memory Cell," *International Electron Devices Meeting Technical Digest*, pp. 331-334, 1995.

15. V. H. Chan and D. Liu, "An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices," *IEEE Electron Devices Letters,* Vol. 20, No. 3, pp. 140-142, 1999.